

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74LVX245F, TC74LVX245FW, TC74LVX245FT

### Octal Bus Transceiver

The TC74LVX245F/ FW/ FT is a high-speed CMOS octal bus transceiver fabricated using silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

These devices are suitable for low-voltage and battery operated systems.

It is intended for two-way asynchronous communication between data busses.

The direction of data transmission is determined by the level of the DIR input. The enable input ( $\bar{G}$ ) can be used to disable the device so that the busses are effectively isolated.

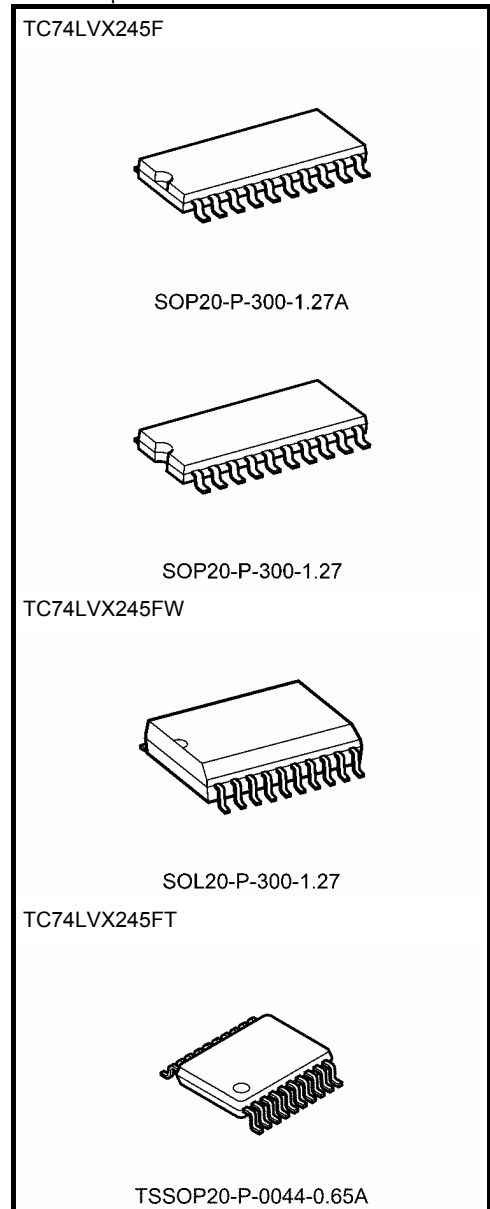
All inputs are equipped with protection circuits against static discharge.

### Features (Note)

- High-speed:  $t_{pd} = 4.7 \text{ ns (typ.)}$  ( $V_{CC} = 3.3 \text{ V}$ )
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max)}$  ( $T_a = 25^\circ\text{C}$ )
- Input voltage level:  $V_{IL} = 0.8 \text{ V (max)}$  ( $V_{CC} = 3 \text{ V}$ )  
 $V_{IH} = 2.0 \text{ V (min)}$  ( $V_{CC} = 3 \text{ V}$ )
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Low noise:  $V_{OLP} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74HC245

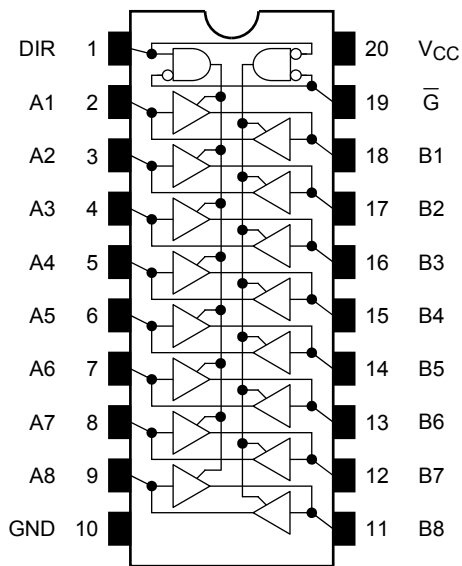
Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.  
All floating (high impedance) bus pins must have their input levels fixed by means of pull-up or pull-down resistors.  
A parasitic diode is formed between the bus and  $V_{CC}$  terminals. Therefore bus terminal can not be used to interface 5-V to 3-V systems directly.

Note: xxxFW (JEDEC SOP) is not available in Japan.

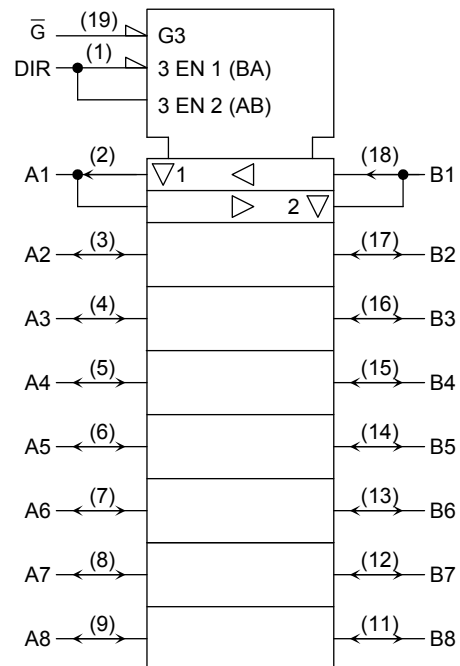


Weight	
SOP20-P-300-1.27A	: 0.22 g (typ.)
SOP20-P-300-1.27	: 0.22 g (typ.)
SOL20-P-300-1.27	: 0.46 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

## Pin Assignment (top view)



## IEC Logic Symbol



## Truth Table

Inputs		Outputs	Function	
$\bar{G}$	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High impedance	

X: Don't care

Z: High impedance

## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage (DIR, $\bar{G}$ )	$V_{IN}$	-0.5 to 7.0	V
DC bus I/O voltage	$V_{I/O}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	±20	mA
DC output current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /ground current	$I_{CC}$	±75	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

## Operating Range (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 3.6	V
Input voltage (DIR, $\bar{G}$ )	$V_{IN}$	0 to 5.5	V
Bus I/O voltage	$V_{I/O}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The operating range is required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either VCC or GND. Please connect both bus inputs and the bus outputs with VCC or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

## Electrical Characteristics

### DC Characteristics

Characteristics		Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max	
Input voltage	H-level	$V_{IH}$	—	2.0	1.5	—	—	1.5	—	V	
				3.0	2.0	—	—	2.0	—		
				3.6	2.4	—	—	2.4	—		
	L-level	$V_{IL}$	—	2.0	—	—	0.5	—	0.5		
				3.0	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output voltage	H-level	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	2.0	—	1.9	—	V
				$I_{OH} = -50 \mu A$	3.0	2.9	3.0	—	2.9	—	
				$I_{OH} = -4 mA$	3.0	2.58	—	—	2.48	—	
	L-level	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0	0.1	—	0.1	
				$I_{OL} = 50 \mu A$	3.0	—	0	0.1	—	0.1	
				$I_{OL} = 4 mA$	3.0	—	—	0.36	—	0.44	
3-State output Off-state current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	3.6	—	—	±0.25	—	±2.5	μA		
Input leakage current	$I_{IN}$	$V_{IN} = 5.5 V$ or GND	3.6	—	—	±0.1	—	±1.0	μA		
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	3.6	—	—	4.0	—	40.0	μA		

## AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max		Min	Max
Propagation delay time	t <sub>pLH</sub>	—	2.7	15	—	6.1	10.7	1.0	13.5	ns
				50	—	8.6	14.2	1.0	17.0	
	3.3 ± 0.3		15	—	4.7	6.6	1.0	8.0		
			50	—	7.2	10.1	1.0	11.5		
Output enable time	t <sub>pZL</sub>	R <sub>L</sub> = 1 kΩ	2.7	15	—	9.0	16.9	1.0	20.5	ns
				50	—	11.5	20.4	1.0	24.0	
	3.3 ± 0.3		15	—	7.1	11.0	1.0	13.0		
			50	—	9.6	14.5	1.0	16.5		
Output disable time	t <sub>pLZ</sub>	R <sub>L</sub> = 1 kΩ	2.7	50	—	11.5	18.0	1.0	21.0	ns
	t <sub>pHZ</sub>		3.3 ± 0.3	50	—	9.6	12.8	1.0	14.5	
Output to output skew	t <sub>osLH</sub>	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t <sub>osHL</sub>		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C <sub>IN</sub>	DIR, $\bar{G}$	(Note 2)		—	4	10	—	10	pF
Bus input capacitance	C <sub>I/O</sub>	An, Bn			—	8	—	—	—	pF
Power dissipation capacitance	C <sub>PD</sub>			(Note 3)	—	21	—	—	—	pF

Note 1: Parameter guaranteed by design.  
 ( $t_{osLH} = |t_{pLHm} - t_{pLHn}|$ ,  $t_{osHL} = |t_{pHLm} - t_{pHLn}|$ )

Note 2: Parameter guaranteed by design.

Note 3: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

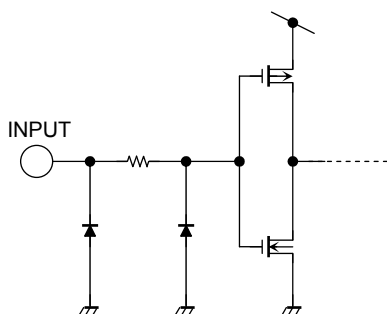
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

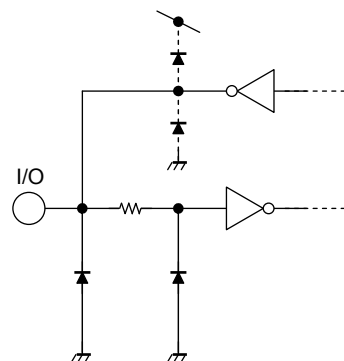
## Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, C<sub>L</sub> = 50 pF)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Limit	Unit
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	—	3.3	-0.5	-0.8	V
Minimum high level dynamic input voltage V <sub>IHD</sub>	V <sub>IHD</sub>	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V <sub>ILD</sub>	V <sub>ILD</sub>	—	3.3	—	0.8	V

### Input Equivalent Circuit



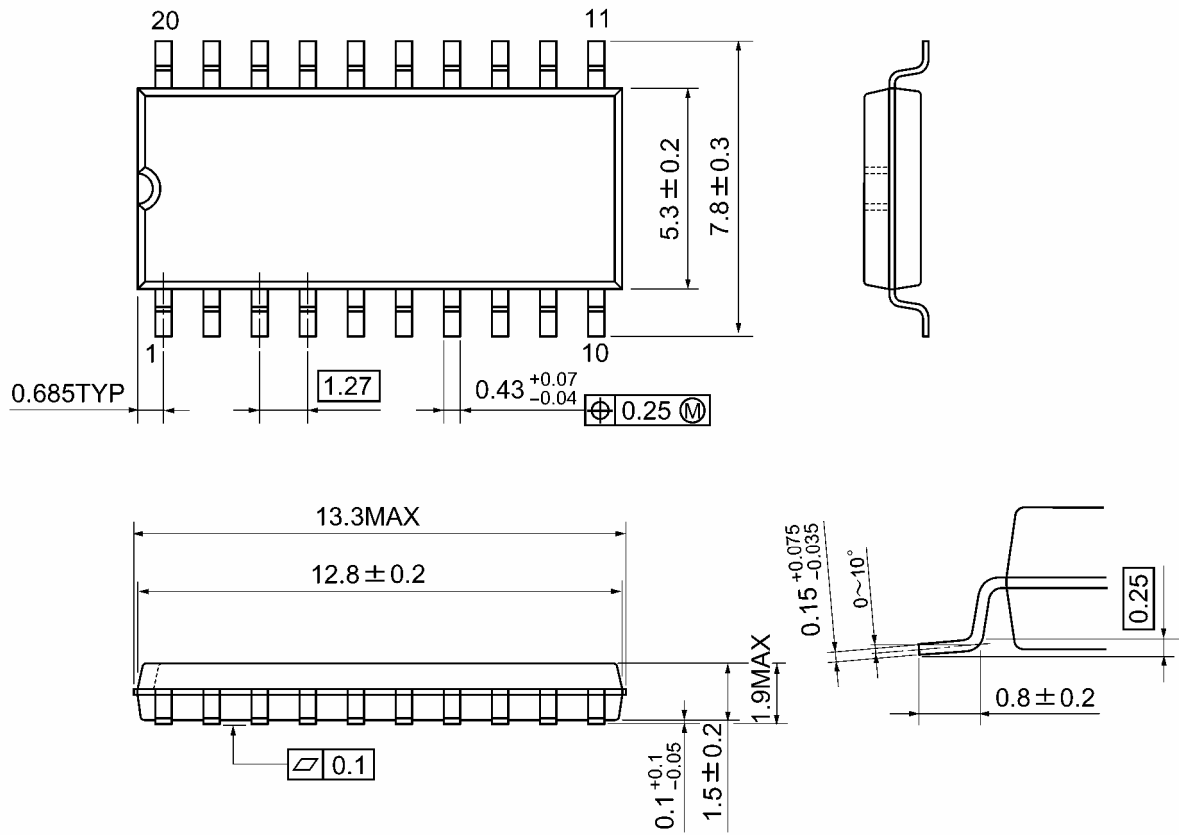
### Bus Terminal Equivalent Circuit (An, Bn)



## Package Dimensions

SOP20-P-300-1.27A

Unit: mm

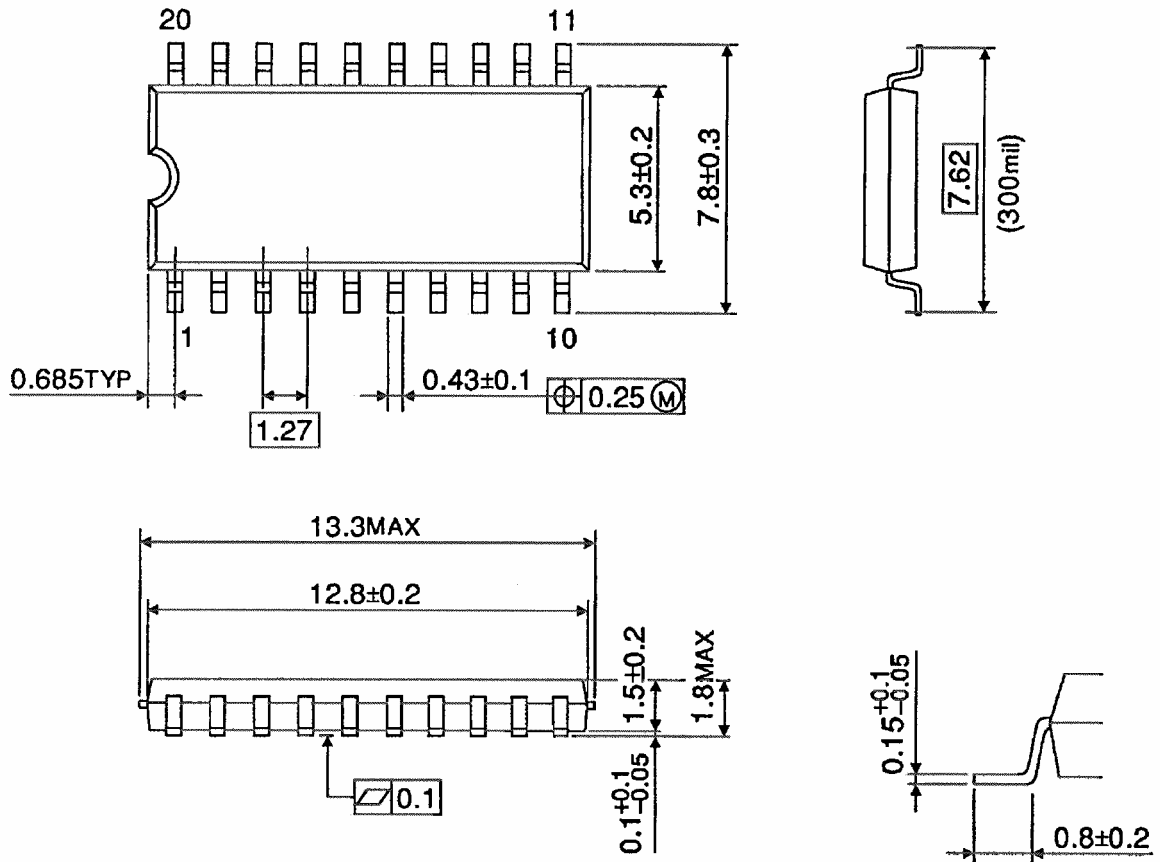


Weight: 0.22 g (typ.)

**Package Dimensions**

SOP20-P-300-1.27

Unit : mm

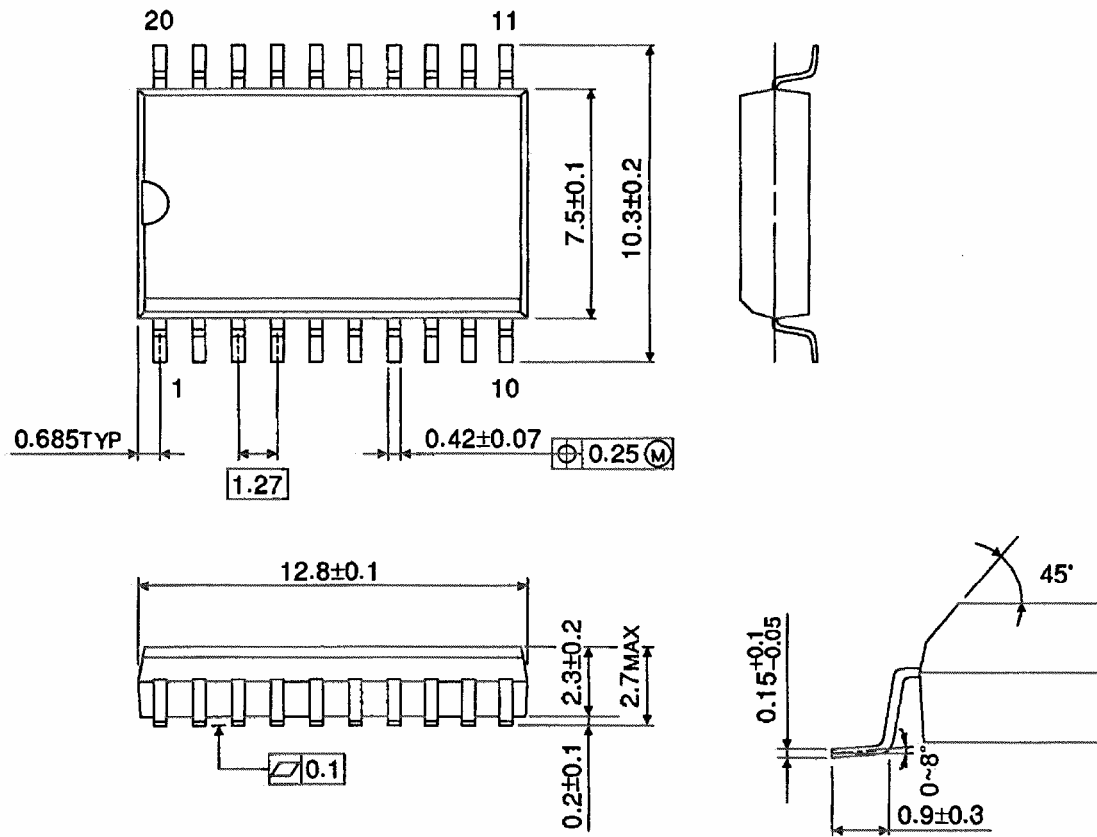


Weight: 0.22 g (typ.)

**Package Dimensions (Note)**

SOL20-P-300-1.27

Unit : mm



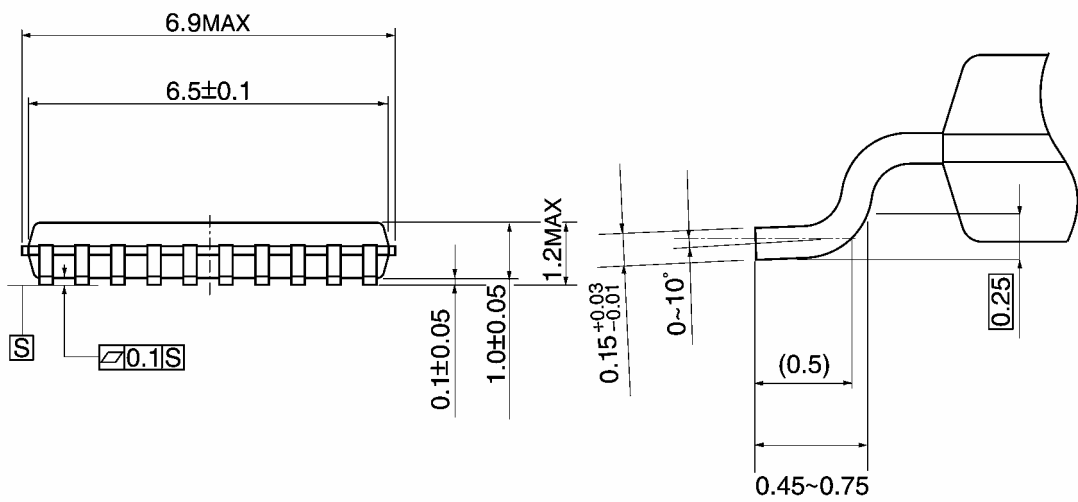
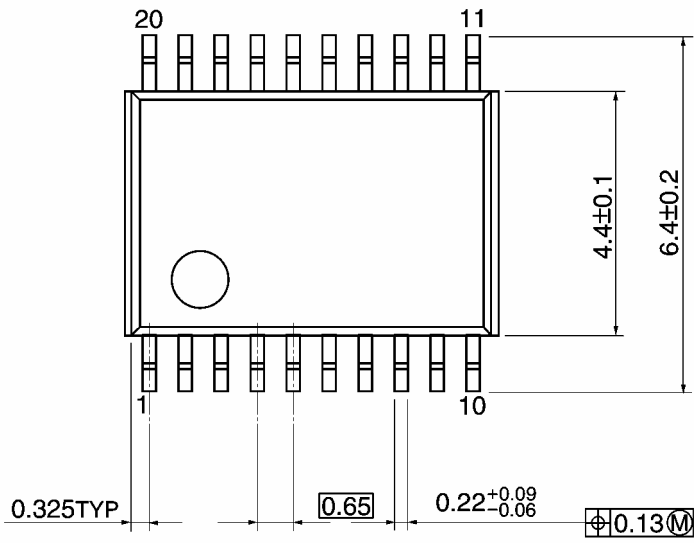
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

**Package Dimensions**

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)



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